74HC164; 74HCT164
8-bit serial-in, parallel-out shift register

1. General description

The 74HC164; 74HCT164 are high-speed Si-gate CMOS devices and are pin compatible with Low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC164; 74HCT164 are 8-bit edge-triggered shift registers with serial data entry and an output from each of the eight stages. Data is entered serially through one of two inputs (DSA or DSB); either input can be used as an active HIGH enable for data entry through the other input. Both inputs must be connected together or an unused input must be tied HIGH.

Data shifts one place to the right on each LOW-to-HIGH transition of the clock (CP) input and enters into Q0, which is the logical AND of the two data inputs (DSA and DSB) that existed one set-up time prior to the rising clock edge.

A LOW level on the master reset ($\overline{MR}$) input overrides all other inputs and clears the register asynchronously, forcing all outputs LOW.

2. Features

- Gated serial data inputs
- Asynchronous master reset
- Complies with JEDEC standard no. 7A
- ESD protection:
    - HBM EIA/JESD22-A114-B exceeds 2000 V
    - MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C.

3. Quick reference data

Table 1: Quick reference data
GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC164						
t_{PHL}, t_{PLH}	propagation delay					
	CP to Qn	C_L = 15 pF; V_{CC} = 5 V	-	12	-	ns
	$\overline{MR}$ to Qn	C_L = 15 pF; V_{CC} = 5 V	-	11	-	ns

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Table 1:   Quick reference data …continued

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{max}	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V	-	78	-	MHz
C_I	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance per package	[1] [2]	-	40	-	pF
Type 74HCT164						
t_{PHL}, t_{PLH}	propagation delay					
	CP to Qn	C_L = 15 pF; V_{CC} = 5 V	-	14	-	ns
	$\overline{MR}$ to Qn	C_L = 15 pF; V_{CC} = 5 V	-	16	-	ns
f_{max}	maximum clock frequency	C_L = 15 pF; V_{CC} = 5 V	-	61	-	MHz
C_I	input capacitance		-	3.5	-	pF
C_{PD}	power dissipation capacitance per package	[1] [3]	-	40	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz

f_o = output frequency in MHz

N = number of inputs switching

$\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

[2]   For HC the condition is V_I = GND to V_{CC}.

[3]   For HCT the condition is V_I = GND to V_{CC} − 1.5 V.

4. Ordering information

Table 2:   Ordering information

Type number	Package				
	Temperature range	Name	Description		Version
74HC164N	−40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)		SOT27-1
74HC164D	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm; body thickness 1.47 mm		SOT108-2
74HC164DB	−40 °C to +125 °C	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm		SOT337-1
74HC164PW	−40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm		SOT402-1
74HCT164N	−40 °C to +125 °C	DIP14	plastic dual in-line package; 14 leads (300 mil)		SOT27-1
74HCT164D	−40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm; body thickness 1.47 mm		SOT108-2

Table 3: **Pin description** …*continued*

Symbol	Pin	Description
GND	7	ground (0 V)
CP	8	clock input (LOW-to-HIGH, edge-triggered)
$\overline{MR}$	9	master reset input (active LOW)
Q4	10	output
Q5	11	output
Q6	12	output
Q7	13	output
V_{CC}	14	positive supply voltage

7. Functional description

7.1 Function selection

Table 4: **Function table** [1]

Operating modes	Input				Output	
	$\overline{MR}$	CP	DSA	DSB	Q0	Q1 to Q7
Reset (clear)	L	X	X	X	L	L to L
Shift	H	↑	l	l	L	q0 to q6
	H	↑	l	h	L	q0 to q6
	H	↑	h	l	L	q0 to q6
	H	↑	h	h	H	q0 to q6

[1] H = HIGH voltage level

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

L = LOW voltage level

l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

q = lower case letters indicate the state of the referenced input one set-up time prior to the LOW-to-HIGH clock transition

↑ = LOW-to-HIGH clock transition

8. Limiting values

Table 5: **Limiting values**
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
I_{IK}	input diode current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output diode current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output source or sink current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V	-	±25	mA
I_{CC}, I_{GND}	V_{CC} or GND current		-	±50	mA
T_{stg}	storage temperature		−65	+150	°C

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Table 5:   Limiting values *…continued*

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
P_{tot}	total power dissipation				
	DIP14 package		[1] -	750	mW
	SO14; SSOP14; TSSOP14; DHVQFN14 package		[2] -	500	mW

[1]   For DIP14 packages: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2]   For SO14 packages: P_{tot} derates linearly with 8 mW/K above 70 °C.

For SSOP14 and TSSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9.   Recommended operating conditions

Table 6:   Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Type 74HC164						
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall time	V_{CC} = 2.0 V	-	-	1000	ns
		V_{CC} = 4.5 V	-	6.0	500	ns
		V_{CC} = 6.0 V	-	-	400	ns
T_{amb}	ambient temperature		−40	-	+125	°C
Type 74HCT164						
V_{CC}	supply voltage		4.5	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
t_r, t_f	input rise and fall time	V_{CC} = 4.5 V	-	6.0	500	ns
T_{amb}	ambient temperature		−40	-	+125	°C

10. Static characteristics

Table 7:   Static characteristics for 74HC164

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V

Table 7:   Static characteristics for 74HC164 …continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −20 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = −20 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = −20 µA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	µA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	µA

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Table 7: **Static characteristics for 74HC164** *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}		-		
		I_O = 20 μA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	μA

Table 8: **Static characteristics for 74HCT164**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = −4 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 4 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
I_{LI}	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	μA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	μA
ΔI_{CC}	additional quiescent supply current per input pin	$V_I = V_{CC}$ − 2.1 V; other inputs $V_I = V_{CC}$ or GND; V_{CC} = 4.5 V to 5.5 V; I_O = 0 A	-	100	360	μA
C_I	input capacitance		-	3.5	-	pF

Table 8: **Static characteristics for 74HCT164** *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).
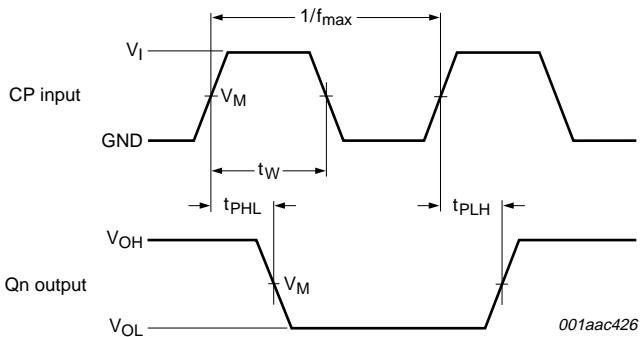
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T$_{amb}$ = −40 °C to +85 °C						
V$_{IH}$	HIGH-level input voltage	V$_{CC}$ = 4.5 V to 5.5 V	2.0	-	-	V
V$_{IL}$	LOW-level input voltage	V$_{CC}$ = 4.5 V to 5.5 V	-	-	0.8	V
V$_{OH}$	HIGH-level output voltage	V$_I$ = V$_{IH}$ or V$_{IL}$				
		I$_O$ = −20 µA; V$_{CC}$ = 4.5 V	4.4	-	-	V
		I$_O$ = −4 mA; V$_{CC}$ = 4.5 V	3.84	-	-	V
V$_{OL}$	LOW-level output voltage	V$_I$ = V$_{IH}$ or V$_{IL}$				
		I$_O$ = 20 µA; V$_{CC}$ = 4.5 V	-	-	0.1	V
		I$_O$ = 4 mA; V$_{CC}$ = 4.5 V	-	-	0.33	V
I$_{LI}$	input leakage current	V$_I$ = V$_{CC}$ or GND; V$_{CC}$ = 5.5 V	-	-	±1.0	µA
I$_{CC}$	quiescent supply current	V$_I$ = V$_{CC}$ or GND; I$_O$ = 0 A; V$_{CC}$ = 5.5 V	-	-	80.0	µA
ΔI$_{CC}$	additional quiescent supply current per input pin	V$_I$ = V$_{CC}$ − 2.1 V; other inputs V$_I$ = V$_{CC}$ or GND; V$_{CC}$ = 4.5 V to 5.5 V; I$_O$ = 0 A	-	-	450	µA
T$_{amb}$ = −40 °C to +125 °C						
V$_{IH}$	HIGH-level input voltage	V$_{CC}$ = 4.5 V to 5.5 V	2.0	-	-	V
V$_{IL}$	LOW-level input voltage	V$_{CC}$ = 4.5 V to 5.5 V	-	-	0.8	V
V$_{OH}$	HIGH-level output voltage	V$_I$ = V$_{IH}$ or V$_{IL}$				
		I$_O$ = −20 µA; V$_{CC}$ = 4.5 V	4.4	-	-	V
		I$_O$ = −4 mA; V$_{CC}$ = 4.5 V	3.7	-	-	V
V$_{OL}$	LOW-level output voltage	V$_I$ = V$_{IH}$ or V$_{IL}$				
		I$_O$ = 20 µA; V$_{CC}$ = 4.5 V	-	-	0.1	V
		I$_O$ = 4 mA; V$_{CC}$ = 4.5 V	-	-	0.4	V
I$_{LI}$	input leakage current	V$_I$ = V$_{CC}$ or GND; V$_{CC}$ = 5.5 V	-	-	±1.0	µA
I$_{CC}$	quiescent supply current	V$_I$ = V$_{CC}$ or GND; I$_O$ = 0 A; V$_{CC}$ = 5.5 V	-	-	160.0	µA
ΔI$_{CC}$	additional quiescent supply current per input pin	V$_I$ = V$_{CC}$ − 2.1 V; other inputs V$_I$ = V$_{CC}$ or GND; V$_{CC}$ = 4.5 V to 5.5 V; I$_O$ = 0 A	-	-	490	µA

Table 10:   Dynamic characteristics for 74HCT164

*GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; test circuit see Figure 10; unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	V_{CC} = 4.5 V; see Figure 7	-	17	36	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	V_{CC} = 4.5 V; see Figure 8	-	19	38	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; see Figure 7	-	7	15	ns
t_W	clock pulse width; HIGH or LOW	V_{CC} = 4.5 V; see Figure 7	18	7	-	ns
	master reset pulse width; LOW	V_{CC} = 4.5 V; see Figure 8	18	10	-	ns
t_{rem}	removal time $\overline{MR}$ to CP	V_{CC} = 4.5 V; see Figure 8	16	7	-	ns
t_{su}	set-up time DSA, and DSB to CP	V_{CC} = 4.5 V; see Figure 9	12	6	-	ns
t_h	hold time DSA, and DSB to CP	V_{CC} = 4.5 V; see Figure 9	+4	−2	-	ns
f_{max}	maximum clock pulse frequency	V_{CC} = 4.5 V; see Figure 7	27	55	-	MHz
T_{amb} = −40 °C to +85 °C						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	V_{CC} = 4.5 V; see Figure 7	-	-	45	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	V_{CC} = 4.5 V; see Figure 8	-	-	48	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; see Figure 7	-	-	19	ns
t_W	clock pulse width; HIGH or LOW	V_{CC} = 4.5 V; see Figure 7	23	-	-	ns
	master reset pulse width; LOW	V_{CC} = 4.5 V; see Figure 8	23	-	-	ns
t_{rem}	removal time $\overline{MR}$ to CP	V_{CC} = 4.5 V; see Figure 8	20	-	-	ns
t_{su}	set-up time DSA, and DSB to CP	V_{CC} = 4.5 V; see Figure 9	15	-	-	ns
t_h	hold time DSA, and DSB to CP	V_{CC} = 4.5 V; see Figure 9	4	-	-	ns
f_{max}	maximum clock pulse frequency	V_{CC} = 4.5 V; see Figure 7	22	-	-	MHz
T_{amb} = −40 °C to +125 °C						
t_{PHL}, t_{PLH}	propagation delay CP to Qn	V_{CC} = 4.5 V; see Figure 7	-	-	54	ns
t_{PHL}	propagation delay $\overline{MR}$ to Qn	V_{CC} = 4.5 V; see Figure 8	-	-	57	ns
t_{THL}, t_{TLH}	output transition time	V_{CC} = 4.5 V; see Figure 7	-	-	22	ns

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8-bit serial-in, parallel-out shift register

Table 10: Dynamic characteristics for 74HCT164 …*continued*
GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF; test circuit see Figure 10; unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_W	clock pulse width; HIGH or LOW	$V_{CC} = 4.5$ V; see Figure 7	27	-	-	ns
	master reset pulse width; LOW	$V_{CC} = 4.5$ V; see Figure 8	27	-	-	ns
t_{rem}	removal time $\overline{MR}$ to CP	$V_{CC} = 4.5$ V; see Figure 8	24	-	-	ns
t_{su}	set-up time DSA and DSB to CP	$V_{CC} = 4.5$ V; see Figure 9	18	-	-	ns
t_h	hold time DSA and DSB to CP	$V_{CC} = 4.5$ V; see Figure 9	4	-	-	ns
f_{max}	maximum clock pulse frequency	$V_{CC} = 4.5$ V; see Figure 7	18	-	-	MHz
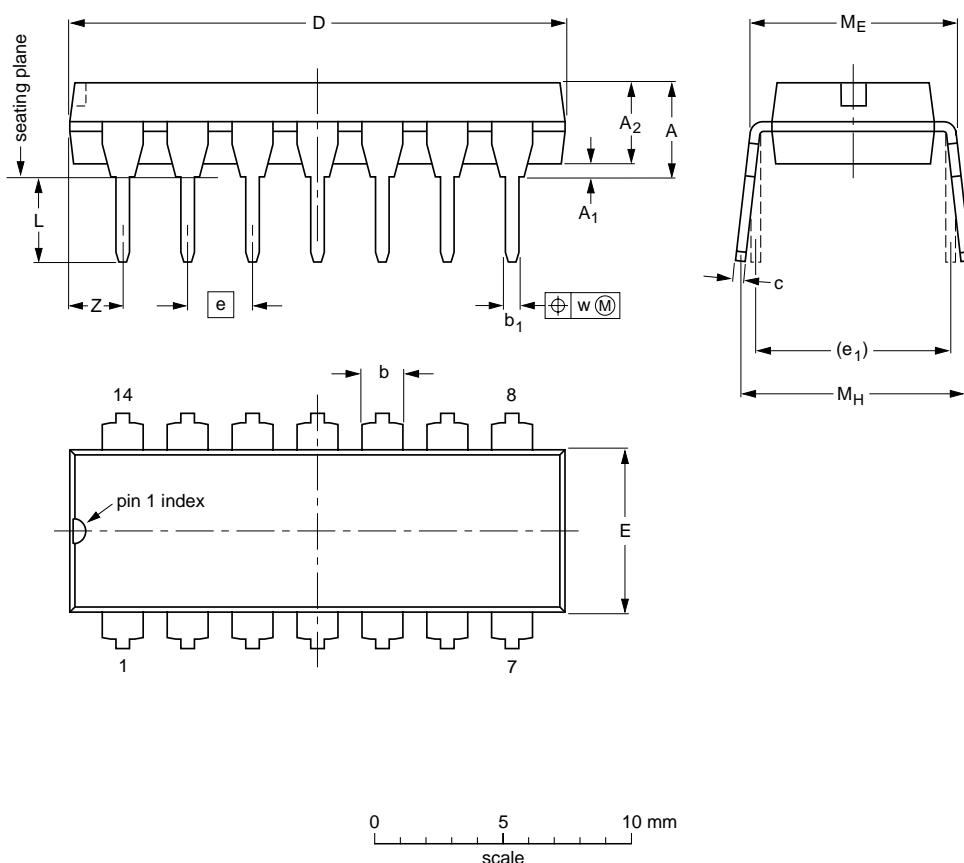
(1) 74HC164: $V_M = 50$ %; $V_I = $ GND to V_{CC}.

74HCT164: $V_M = 1.3$ V; $V_I = $ GND to 3 V.

Fig 7. Waveforms showing the clock (CP) to output (Qn) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency

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12. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A$_1$ min.	A$_2$ max.	b	b$_1$	c	D$^{(1)}$	E$^{(1)}$	e	e$_1$	L	M$_E$	M$_H$	w	Z$^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	
	IEC	JEDEC	JEITA		
SOT27-1	050G04	MO-001	SC-501-14		

Fig 11. Package outline SOT27-1 (DIP14)